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Iwasaki, K.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 7 , Issue: 1 , Jan. 1988

Pages:84 - 90

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2 A flexible logic BIST scheme and its application to SoC designs

Xiaoqing Wen; Hsin-Po Wang;

Test Symposium, 2001. Proceedings. 10th Asian , 19-21 Nov. 2001

Pages:463

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3 A cost-effective scheme for at-speed self-test

Xiaowei Li; Fuqing Yang;

TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering.1993 IEEE Region 10 Conference on , Issue: 0 , 19-21 Oct. 1993

Pages:89 - 92 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(192 KB\)\]](#) **IEEE CNF**

4 Self-testing and self-reconfiguration architecture for 2-D WSI arrays

Abujbara, H.Y.; Al-Arian, S.A.;

Parallel and Distributed Processing, 1990. Proceedings of the Second IEEE Symposium on , 9-13 Dec. 1990

Pages:527 - 530

[\[Abstract\]](#) [\[PDF Full-Text \(320 KB\)\]](#) **IEEE CNF**

5 E-BIST: enhanced test-per-clock BIST architecture

Son, Y.; Chong, J.; Russell, G.;

Computers and Digital Techniques, IEE Proceedings- , Volume: 149 , Issue:

1 , Jan. 2002

Pages:9 - 15

[\[Abstract\]](#) [\[PDF Full-Text \(571 KB\)\]](#) IEE JNL

6 Scan latch design for delay test

Savir, J.;

Test Conference, 1997. Proceedings., International , 1-6 Nov. 1997

Pages:446 - 453

[\[Abstract\]](#) [\[PDF Full-Text \(592 KB\)\]](#) IEEE CNF

7 The influence of directional sampling on bidirectional reflectance and albedo retrieval using kernel-driven models

Wanner, W.; Lewis, P.; Roujean, J.-L.;

Geoscience and Remote Sensing Symposium, 1996. IGARSS '96. 'Remote Sensing for a Sustainable Future.', International , Volume: 3 , 27-31 May 1996

Pages:1408 - 1410 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(296 KB\)\]](#) IEEE CNF

8 A register-transfer level BIST partitioning approach for ASIC designs

Laurence Tianruo Yang; Muzio, J.;

Communications, Computers and signal Processing, 2001. PACRIM. 2001 IEEE Pacific Rim Conference on , Volume: 1 , 26-28 Aug. 2001

Pages:275 - 278 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) IEEE CNF

9 On shrinking wide compressors

Savir, J.;

VLSI Test Symposium, 1995. Proceedings., 13th IEEE , 30 April-3 May 1995

Pages:108 - 117

[\[Abstract\]](#) [\[PDF Full-Text \(780 KB\)\]](#) IEEE CNF

10 Module level weighted random patterns

Savir, J.;

Test Symposium, 1995., Proceedings of the Fourth Asian , 23-24 Nov. 1995

Pages:274 - 278

[\[Abstract\]](#) [\[PDF Full-Text \(388 KB\)\]](#) IEEE CNF

11 Reed-Solomon codes based novel signature analysis technique for VLSI random access memory testing

Rayapati, V.N.; Mukhedkar, D.;

Circuits and Systems, 1990., IEEE International Symposium on , 1-3 May 1990

Pages:2324 - 2328 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(380 KB\)\]](#) IEEE CNF

12 Built-in test using perturbed deterministic patterns

Wu, D.M.; Waicukauski, J.;

Circuits and Systems, 1990., IEEE International Symposium on , 1-3 May 1990

Pages:2232 - 2235 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(248 KB\)\]](#) IEEE CNF

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